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(57) **ABSTRACT**

An organic light emitting diode (OLED) pixel driving circuit and an OLED display are provided. The OLED pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED. A drain of the third TFT is connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT. A drain of the fifth TFT is connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT. A drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

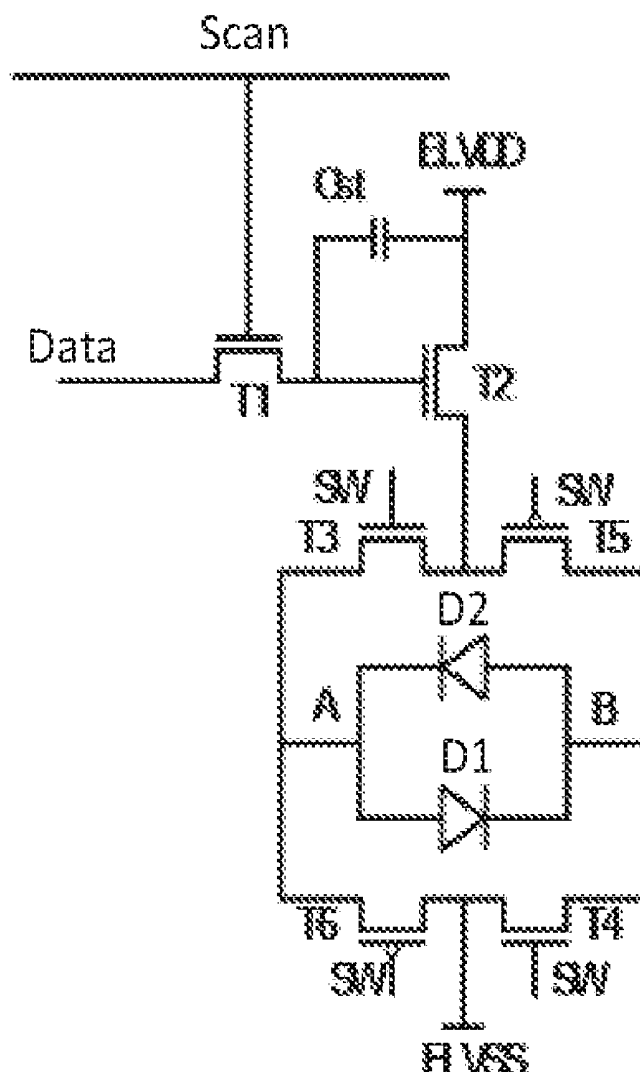
An organic light emitting diode (OLED) pixel driving circuit and an OLED display are provided. The OLED pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED. A drain of the third TFT is connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT. A drain of the fifth TFT is connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT. A drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

An organic light emitting diode (OLED) pixel driving circuit and an OLED display are provided. The OLED pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED. A drain of the third TFT is connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT. A drain of the fifth TFT is connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT. A drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

An organic light emitting diode (OLED) pixel driving circuit and an OLED display are provided. The OLED pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED. A drain of the third TFT is connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT. A drain of the fifth TFT is connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT. A drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

An organic light emitting diode (OLED) pixel driving circuit and an OLED display are provided. The OLED pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED. A drain of the third TFT is connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT. A drain of the fifth TFT is connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT. A drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

An organic light emitting diode (OLED) pixel driving circuit and an OLED display are provided. The OLED pixel driving circuit includes a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED. A drain of the third TFT is connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT. A drain of the fifth TFT is connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT. A drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.



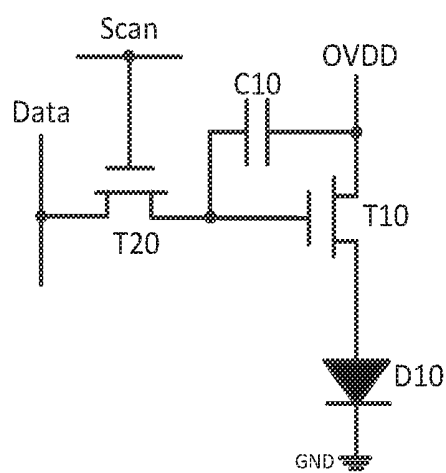


FIG. 1

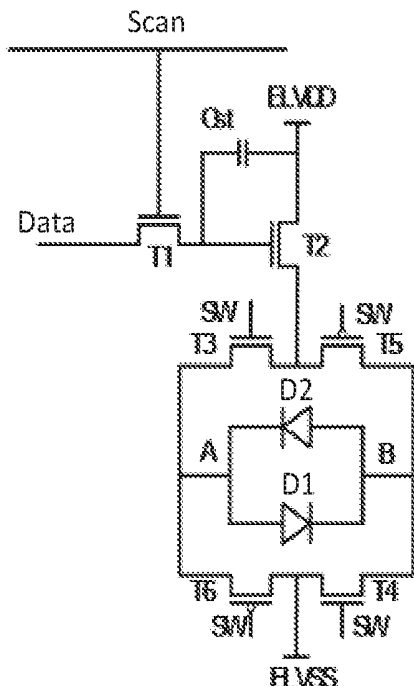


FIG. 2

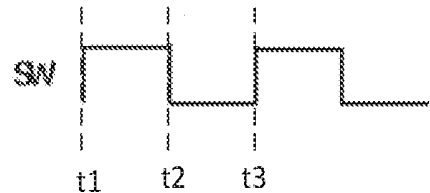


FIG. 3

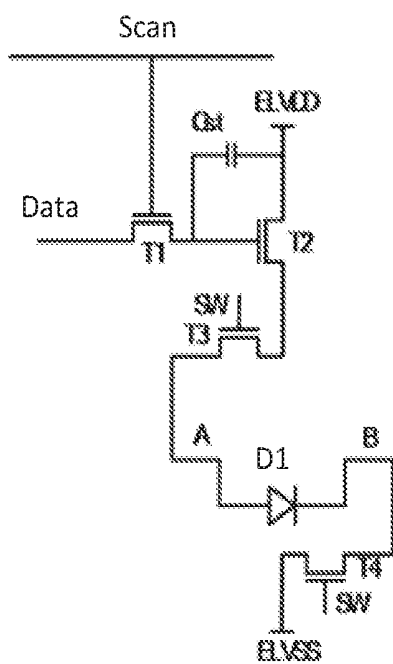


FIG. 4

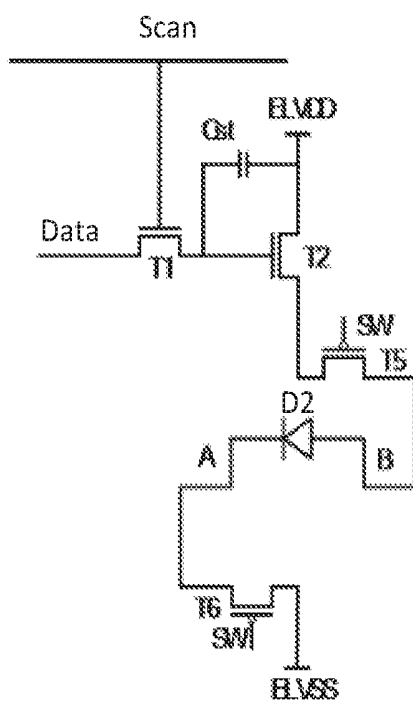


FIG. 5

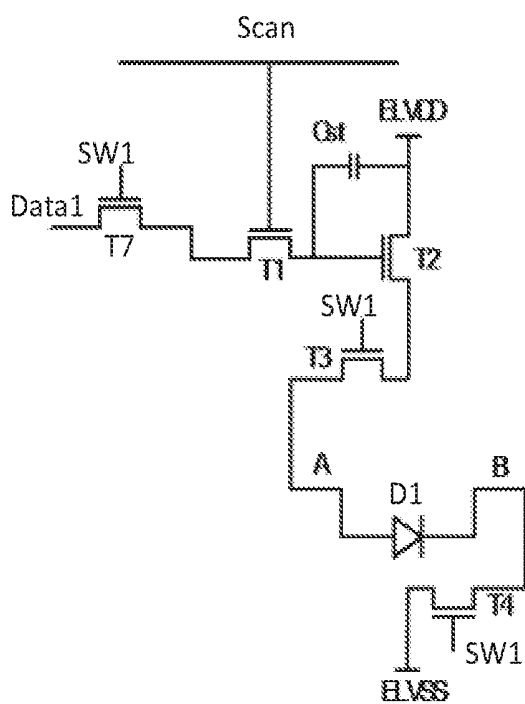


FIG. 8

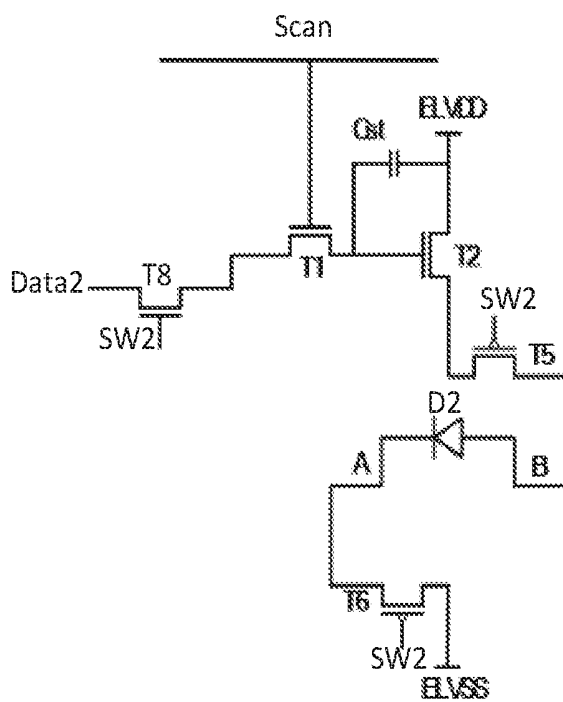


FIG. 9

OLED PIXEL DRIVING CIRCUIT AND OLED DISPLAY

BACKGROUND

1. Field of the Disclosure

[0001] The present disclosure relates to the field of display technology, and more particularly, to an organic light emitting diode (OLED) pixel driving circuit and an OLED display.

2. Description of the Related Art

[0002] An active-matrix organic light emitting diode (AMOLED) is one kind of display technology for televisions and mobile devices. Compared with the mainstream liquid crystal displays (LCDs) of the related art, the AMOLED displays have advantages of high contrast, wide viewing angle, low power consumption, and compact size so the AMOLED is one of the most popular flat panel display technologies.

[0003] However, the brightness of the OLEDs display of the related art keeps the same very long, resulting in the shift of the light-emitting characteristics. In addition, the efficiency of light emitting is lowered so afterimages occur easily and the display effect is lowered.

[0004] To solve the problem of the related art, it is necessary to propose a new OLED pixel driving circuit and an OLED display adopting the OLED pixel driving circuit.

SUMMARY

[0005] An object of the present disclosure is to propose a solution, that is, to provide an organic light emitting diode (OLED) pixel driving circuit and an OLED display. Afterimages are eliminated and the displaying effect is improved in the present disclosure.

[0006] According to a first aspect of the present disclosure, an organic light emitting diode (OLED) pixel driving circuit includes:

[0007] a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED;

[0008] a gate of the first TFT receiving a scanning signal; a source of the first TFT receiving a data signal; a drain of the first TFT connected to a gate of the second TFT and one terminal of the capacitor;

[0009] a source of the second TFT and the other terminal of the capacitor both receiving a power supply positive voltage; a drain of the second TFT connected to a source of the third TFT and a source of the fifth TFT;

[0010] a gate of the third TFT, a gate of the fourth TFT, a gate of the fifth TFT, and a gate of the sixth TFT all receiving a controlling signal; a drain of the third TFT connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT;

[0011] a drain of the fifth TFT connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT;

[0012] a drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage;

[0013] wherein the first TFT, the second TFT, the third TFT, and the fourth TFT are all N-type TFTs; the fifth TFT and the sixth TFT are both P-type TFTs; when a current frame of image is displayed, the controlling signal is at a

high voltage level; when a following frame of image is displayed, the controlling signal is at a low voltage level.

[0014] According to an embodiment of the present disclosure, the OLED pixel driving circuit further comprises a seventh TFT and an eighth TFT; the controlling signal comprises a first controlling signal and a second controlling signal; the data signal comprises a first data signal and a second data signal;

[0015] a gate of the seventh TFT receives the first controlling signal; a source of the seventh TFT receives the first data signal;

[0016] a gate of the eighth TFT receives a second controlling signal; a source of the eighth TFT receives a second data signal; the source of the first TFT is connected to a drain of the seventh TFT and a drain of the eighth TFT;

[0017] the gate of the third TFT and the gate of the fourth TFT both receive the first controlling signal;

[0018] the gate of the fifth TFT and the gate of the sixth TFT both receive the second controlling signal.

[0019] According to an embodiment of the present disclosure, the seventh TFT and the eighth TFT are both N-type TFTs.

[0020] According to an embodiment of the present disclosure, when the current frame of image is displayed, the first controlling signal is at a high voltage level and the second controlling signal is at a low voltage level; when the following frame of image is displayed, the second controlling signal is at a high voltage level and the first controlling signal is at a low voltage level.

[0021] According to an embodiment of the present disclosure, the first controlling signal and the second controlling signal are both signals with a square wave; the period of the first controlling signal is the same as the period of the second controlling signal; the polarity of the first controlling signal is opposite to the polarity of the second controlling signal.

[0022] According to an embodiment of the present disclosure, the first data signal and the second data signal are set according to the brightness of the first OLED and the brightness of the second OLED at the same grayscale level; the brightness of the first OLED is the same as the brightness of the second OLED at the same grayscale level.

[0023] According to an embodiment of the present disclosure, the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT, and the sixth TFT all are low temperature polysilicon TFTs, oxide semiconductor TFTs, or amorphous silicon (a-Si) TFTs arbitrarily.

[0024] According to a second aspect of the present disclosure, an organic light emitting diode (OLED) pixel driving circuit comprises:

[0025] a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED;

[0026] a gate of the first TFT receiving a scanning signal; a source of the first TFT receiving a data signal; a drain of the first TFT connected to a gate of the second TFT and one terminal of the capacitor;

[0027] a source of the second TFT and the other terminal of the capacitor both receiving a power supply positive voltage; a drain of the second TFT connected to a source of the third TFT and a source of the fifth TFT;

[0028] a gate of the third TFT, a gate of the fourth TFT, a gate of the fifth TFT, and a gate of the sixth TFT all receiving

a controlling signal; a drain of the third TFT connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT;

[0029] a drain of the fifth TFT connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT;

[0030] a drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

[0031] According to an embodiment of the present disclosure, the first TFT, the second TFT, the third TFT, and the fourth TFT are all N-type TFTs; the fifth TFT and the sixth TFT are both P-type TFTs.

[0032] According to an embodiment of the present disclosure, when a current frame of image is displayed, the controlling signal is at a high voltage level; when a following frame of image is displayed, the controlling signal is at a low voltage level.

[0033] According to an embodiment of the present disclosure, the OLED pixel driving circuit further comprises a seventh TFT and an eighth TFT; the controlling signal comprises a first controlling signal and a second controlling signal; the data signal comprises a first data signal and a second data signal;

[0034] a gate of the seventh TFT receives the first controlling signal; a source of the seventh TFT receives the first data signal;

[0035] a gate of the eighth TFT receives a second controlling signal; a source of the eighth TFT receives a second data signal; the source of the first TFT is connected to a drain of the seventh TFT and a drain of the eighth TFT;

[0036] the gate of the third TFT and the gate of the fourth TFT both receive the first controlling signal;

[0037] the gate of the fifth TFT and the gate of the sixth TFT both receive the second controlling signal.

[0038] According to an embodiment of the present disclosure, the seventh TFT and the eighth TFT are both N-type TFTs.

[0039] According to an embodiment of the present disclosure, when the current frame of image is displayed, the first controlling signal is at a high voltage level and the second controlling signal is at a low voltage level; when the following frame of image is displayed, the second controlling signal is at a high voltage level and the first controlling signal is at a low voltage level.

[0040] According to an embodiment of the present disclosure, the first controlling signal and the second controlling signal are both signals with a square wave; the period of the first controlling signal is the same as the period of the second controlling signal; the polarity of the first controlling signal is opposite to the polarity of the second controlling signal.

[0041] According to an embodiment of the present disclosure, the first data signal and the second data signal are set according to the brightness of the first OLED and the brightness of the second OLED at the same grayscale level; the brightness of the first OLED is the same as the brightness of the second OLED at the same grayscale level.

[0042] According to an embodiment of the present disclosure, the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT, and the sixth TFT all are low temperature polysilicon TFTs, oxide semiconductor TFTs, or amorphous silicon (a-Si) TFTs arbitrarily.

[0043] According to a third aspect of the present disclosure, an organic light emitting diode (OLED) display includes an OLED pixel driving circuit as disclosed above.

[0044] The OLED pixel driving circuit and the OLED display of the present disclosure prevent the OLED from being in a light-emitting state very long and avoid the shift of the light-emitting characteristics of the OLED by means of reversing bias frame-by-frame, thereby eliminating the afterimage phenomenon and improving the display effect of the panel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0045] FIG. 1 illustrates an organic light emitting diode (OLED) pixel driving circuit of the related art.

[0046] FIG. 2 illustrates a circuit diagram of the OLED pixel driving circuit according to an embodiment of the present disclosure.

[0047] FIG. 3 illustrates a waveform of a controlling signal applied in the OLED pixel driving circuit according to an embodiment of the present disclosure.

[0048] FIG. 4 illustrates an equivalent circuit of the OLED pixel driving circuit depicted in FIG. 2 when displaying a current frame.

[0049] FIG. 5 illustrates an equivalent circuit of the OLED pixel driving circuit depicted in FIG. 2 when displaying a next frame.

[0050] FIG. 6 illustrates a circuit diagram of the OLED pixel driving circuit according to another embodiment of the present disclosure.

[0051] FIG. 7 illustrates a waveform of a controlling signal applied in the OLED pixel driving circuit depicted in FIG. 6.

[0052] FIG. 8 illustrates an equivalent circuit of the OLED pixel driving circuit depicted in FIG. 6 when displaying a current frame.

[0053] FIG. 9 illustrates an equivalent circuit of the OLED pixel driving circuit depicted in FIG. 6 when displaying a next frame.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0054] Spatially relative terms, such as “beneath”, “below”, “lower”, “above”, “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures.

[0055] The structure of an organic light emitting diode (OLED) pixel driving circuit of the related art is usually 2T1C, that is, the structure of two thin-film transistors (TFTs) and a capacitor. The OLED pixel driving circuit of the related art converts voltage into the current. As illustrated in FIG. 1, the OLED pixel driving circuit with the 2T1C structure of the related art includes a first TFT T10, a second TFT T20, a capacitor C10, and an OLED D10. The first TFT T10 is a driving TFT. The second TFT T20 is a switching TFT. The capacitor C10 is a storage capacitor. A gate of the second TFT T20 receives a scanning signal Scan. A source of the second TFT T20 receives a data signal Data. A drain of the second TFT T20 is electrically connected to a gate of the first TFT T10. A source of the first TFT T10 receives a power supply positive voltage OVDD. A drain of the first TFT T10 is electrically connected to an anode of the OLED D10. A cathode of the OLED D10 is grounded. One

terminal of the capacitor C10 is electrically connected to the gate of the first TFT T10. The other terminal of the capacitor C10 is electrically connected to the source of the first TFT T10.

[0056] When the 2T1C pixel driving circuit drives the OLED, the current flowing through the OLED D10 satisfies a formula as follows:

$$I=k\alpha(V_{gs}-V_{th})^2;$$

[0057] In this formula, I represents the current flowing through the OLED D10; k represents an intrinsic conductive factor of the driving TFT; V_{gs} represents the difference between voltage imposed on the gate of the first TFT T10 and voltage imposed on the source of the first TFT T10; V_{th} represents the threshold voltage imposed on the first TFT T10.

[0058] Please refer to FIG. 2 to FIG. 9. FIG. 2 illustrates a schematic diagram of the OLED pixel driving circuit according to an embodiment of the present disclosure.

[0059] As illustrated in FIG. 2, the OLED pixel driving circuit of the present disclosure includes a first TFT T1, a second TFT T2, a third TFT T3, a fourth TFT T4, a fifth TFT T5, a sixth TFT T6, a capacitor Cst, a first OLED D1, and a second OLED D2. The first TFT T1 is a driving TFT. The OLED pixel driving circuit inputs a scanning signal Scan, a data signal Data, and a controlling signal SW.

[0060] Specifically, these components are connected in the following manner: A gate of the first TFT T1 receives the scanning signal Scan. A source of the first TFT T1 receives the data signal Data. A drain of the first TFT T1 is connected to a gate of the second TFT T2 and one terminal of the capacitor Cst.

[0061] A source of the second TFT T2 and the other terminal of the capacitor Cst both receive a power supply positive voltage ELVDD. A drain of the second TFT T2 is connected to a source of the third TFT T3 and a source of the fifth TFT T5.

[0062] A gate of the third TFT T3, a gate of the fourth TFT T4, a gate of the fifth TFT T5, and a gate of the sixth TFT T6 all receive a controlling signal SW. A drain of the third TFT T3 is connected to an anode of the first OLED D1, a cathode of the second OLED D2, and a source of the sixth TFT T6.

[0063] A drain of the fifth TFT T5 is connected to a cathode of the first OLED D1, an anode of the second OLED D2, and a source of the fourth TFT T4;

[0064] A drain of the sixth TFT T6 and a drain of the fourth TFT T4 both receive a power supply negative voltage ELVSS.

[0065] The first TFT T1, the second TFT T2, the third TFT T3, and the fourth TFT T4 are all N-type TFTs. The fifth TFT T5 and the sixth TFT T6 are both P-type TFTs.

[0066] The first TFT T1, the second TFT T2, the third TFT T3, the fourth TFT T4, the fifth TFT T5, and the sixth TFT T6 all are low temperature polysilicon TFTs, oxide semiconductor TFTs, or amorphous silicon (a-Si) TFTs arbitrarily.

[0067] As illustrated in FIG. 3, the controlling signal SW is a signal with a square wave. When a current frame of image (that is, the t1-t2 period) is displayed, the controlling signal SW is at a high voltage level. When a following frame of image is displayed (that is, a t2-t3 period), the controlling signal SW is at a low voltage level. The remaining frames are similar to this condition.

[0068] As illustrated in FIG. 4, when a first frame of image is displayed and the controlling signal SW is at a high voltage level, the third TFT T3 and the fourth TFT T4 are both turned on and the fifth TFT T5 and the sixth TFT T6 are both turned off. At this time, the voltage on node A is greater than the voltage on node B, which drives the first OLED D1 to emit light. In addition, the second OLED D2 is in a reverse bias state.

[0069] As illustrated in FIG. 5, when a second frame of image is displayed and the controlling signal SW is at a low voltage level, the fifth TFT T5 and the sixth TFT T6 are both turned on and the third TFT T3 and the fourth TFT T4 are both turned off. At this time, the voltage on node B is greater than the voltage on node A, which drives the second OLED D2 to emit light. Moreover, the first OLED D1 is in a reverse bias state.

[0070] Therefore, the OLED in the present disclosure avoids keeping emitting light long by means of a frame-by-frame reverse bias and prevents the shift of the light-emitting characteristics of the OLED, effectively prevents the generation of afterimages, and further prolongs the service life of the OLED.

[0071] In order to solve the problem that the luminous efficiencies of the first OLED D1 and the second OLED D2 are inconsistent due to the process differences, that is, the brightness of two adjacent frames flickers inconsistently. As illustrated in FIG. 6, the OLED pixel driving circuit proposed by the present embodiment further includes a seventh TFT T7 and an eighth TFT T8. The controlling signal includes a first controlling signal SW1 and a second controlling signal SW2. The data signal includes a first data signal Data1 and a second data signal Data2. The OLED pixel driving circuit inputs the first data signal Data1, the second data signal Data2, the first controlling signal SW1, and the second controlling signal SW2.

[0072] A gate of the seventh TFT T7 receives the first controlling signal SW1. A source of the seventh TFT T7 receives the first data signal Data1.

[0073] A gate of the eighth TFT T8 receives the second controlling signal SW2. A source of the eighth TFT T8 receives the second data signal Data2. The source of the first TFT T1 is connected to a drain of the seventh TFT T7 and a drain of the eighth TFT T8.

[0074] The gate of the third TFT T3 and the gate of the fourth TFT T4 both receive the first controlling signal SW1. The gate of the fifth TFT T5 and the gate of the sixth TFT T6 both receive the second controlling signal SW2.

[0075] The seventh TFT T7 and the eighth TFT T8 are both N-type TFTs.

[0076] As illustrated in FIG. 7, the first controlling signal SW1 and the second controlling signal SW2 are both signals with a square wave. Moreover, the period of the first controlling signal SW1 is the same as the period of the second controlling signal SW2. However, the polarity of the first controlling signal SW1 is opposite to the polarity of the second controlling signal SW2.

[0077] As illustrated in FIG. 8, when the current frame of image (for example, the first frame of image, that is, the t1-t2 period) is displayed, the first controlling signal SW1 is at a high voltage level and the second controlling signal SW2 is at a low voltage level. Besides, the third TFT T3 and the fourth TFT T4 are both turned on, and the fifth TFT T5 and the sixth TFT T6 are both turned off. At this time, the voltage on node A is greater than the voltage on node B, which

drives the first OLED D1 to emit light. Moreover, the second OLED D2 is in a reverse bias state.

[0078] As illustrated in FIG. 9, when the following frame of image (that is, the t2-t3 period) is displayed, the second controlling signal SW2 is at a high voltage level and the first controlling signal SW1 is at a low voltage level. Besides, the fifth TFT T5 and the sixth TFT T6 are both turned on, and the third TFT T3 and the fourth TFT T4 are both turned off. At this time, the voltage on node B is greater than the voltage on node A, which drives the second OLED D2 to emit light. Moreover, the first OLED D1 is in a reverse bias state.

[0079] The size of the first data signal Data1 and the size of the second data signal Data2 are set according to the brightness of the first OLED D1 and the second OLED D2 at the same grayscale level. The brightness of the first OLED D1 is the same as the brightness of the second OLED D2 at the same grayscale level.

[0080] That is to say, the brightness of the first OLED D1 and the brightness of the second OLED D2 at the same grayscale level are the same by adjusting the size of the first data signal Data1 and the size of the second data signal Data2.

[0081] For example, when the brightness of the first OLED D1 under the testing grayscale is greater than the brightness of the second OLED D2, the first data signal is turned down so that the brightness of the first OLED D1 can be equal to the brightness of the second OLED D2 at the same grayscale level. While the brightness of the first OLED D1 under the testing grayscale is less than the brightness of the second OLED D2, the second data signal is turned down so that the brightness of the first OLED D1 can be equal to the brightness of the second OLED D2 at the same grayscale level.

[0082] The present disclosure further provides an organic light emitting diode (OLED) display including the OLED pixel driving circuit, which has been detailed in the embodiment.

[0083] The OLED pixel driving circuit and the OLED display of the present disclosure prevent the OLED from being in a light-emitting state very long and avoid the shift of the light-emitting characteristics of the OLED by means of reversing bias frame-by-frame, thereby eliminating the afterimage phenomenon and improving the display effect of the panel.

[0084] While the present invention has been described in connection with what is considered the most practical and preferred embodiments, it is understood that this invention is not limited to the disclosed embodiments but is intended to cover various arrangements made without departing from the scope of the broadest interpretation of the appended claims.

What is claimed is:

1. An organic light emitting diode (OLED) pixel driving circuit, comprising:

- a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED;
- a gate of the first TFT receiving a scanning signal; a source of the first TFT receiving a data signal; a drain of the first TFT connected to a gate of the second TFT and one terminal of the capacitor;
- a source of the second TFT and the other terminal of the capacitor both receiving a power supply positive volt-

age; a drain of the second TFT connected to a source of the third TFT and a source of the fifth TFT;

- a gate of the third TFT, a gate of the fourth TFT, a gate of the fifth TFT, and a gate of the sixth TFT all receiving a controlling signal; a drain of the third TFT connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT;

- a drain of the fifth TFT connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT;

- a drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage;

wherein the first TFT, the second TFT, the third TFT, and the fourth TFT are all N-type TFTs; the fifth TFT and the sixth TFT are both P-type TFTs; when a current frame of image is displayed, the controlling signal is at a high voltage level; when a following frame of image is displayed, the controlling signal is at a low voltage level.

2. The OLED pixel driving circuit of claim 1, wherein the OLED pixel driving circuit further comprises a seventh TFT and an eighth TFT; the controlling signal comprises a first controlling signal and a second controlling signal; the data signal comprises a first data signal and a second data signal;

- a gate of the seventh TFT receives the first controlling signal; a source of the seventh TFT receives the first data signal;

- a gate of the eighth TFT receives a second controlling signal; a source of the eighth TFT receives a second data signal; the source of the first TFT is connected to a drain of the seventh TFT and a drain of the eighth TFT;

the gate of the third TFT and the gate of the fourth TFT both receive the first controlling signal;

the gate of the fifth TFT and the gate of the sixth TFT T6 both receive the second controlling signal.

3. The OLED pixel driving circuit of claim 2, wherein the seventh TFT and the eighth TFT are both N-type TFTs.

4. The OLED pixel driving circuit of claim 2, wherein when the current frame of image is displayed, the first controlling signal is at a high voltage level and the second controlling signal is at a low voltage level; when the following frame of image is displayed, the second controlling signal is at a high voltage level and the first controlling signal is at a low voltage level.

5. The OLED pixel driving circuit of claim 2, wherein the first controlling signal and the second controlling signal are both signals with a square wave; the period of the first controlling signal is the same as the period of the second controlling signal; the polarity of the first controlling signal is opposite to the polarity of the second controlling signal.

6. The OLED pixel driving circuit of claim 2, wherein the first data signal and the second data signal are set according to the brightness of the first OLED and the brightness of the second OLED at the same grayscale level; the brightness of the first OLED is the same as the brightness of the second OLED at the same grayscale level.

7. The OLED pixel driving circuit of claim 1, wherein the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT, and the sixth TFT all are low temperature polysilicon TFTs, oxide semiconductor TFTs, or amorphous silicon (a-Si) TFTs arbitrarily.

8. An organic light emitting diode (OLED) pixel driving circuit, comprising:

a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED;

a gate of the first TFT receiving a scanning signal; a source of the first TFT receiving a data signal; a drain of the first TFT connected to a gate of the second TFT and one terminal of the capacitor;

a source of the second TFT and the other terminal of the capacitor both receiving a power supply positive voltage; a drain of the second TFT connected to a source of the third TFT and a source of the fifth TFT;

a gate of the third TFT, a gate of the fourth TFT, a gate of the fifth TFT, and a gate of the sixth TFT all receiving a controlling signal; a drain of the third TFT connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT;

a drain of the fifth TFT connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT;

a drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

9. The OLED pixel driving circuit of claim 8, wherein the first TFT, the second TFT, the third TFT, and the fourth TFT are all N-type TFTs; the fifth TFT and the sixth TFT are both P-type TFTs.

10. The OLED pixel driving circuit of claim 8, wherein when a current frame of image is displayed, the controlling signal is at a high voltage level; when a following frame of image is displayed, the controlling signal is at a low voltage level.

11. The OLED pixel driving circuit of claim 8, wherein the OLED pixel driving circuit further comprises a seventh TFT and an eighth TFT; the controlling signal comprises a first controlling signal and a second controlling signal; the data signal comprises a first data signal and a second data signal;

a gate of the seventh TFT receives the first controlling signal; a source of the seventh TFT receives the first data signal;

a gate of the eighth TFT receives a second controlling signal; a source of the eighth TFT receives a second data signal; the source of the first TFT is connected to a drain of the seventh TFT and a drain of the eighth TFT;

the gate of the third TFT and the gate of the fourth TFT both receive the first controlling signal;

the gate of the fifth TFT and the gate of the sixth TFT T6 both receive the second controlling signal.

12. The OLED pixel driving circuit of claim 11, wherein the seventh TFT and the eighth TFT are both N-type TFTs.

13. The OLED pixel driving circuit of claim 11, wherein when the current frame of image is displayed, the first controlling signal is at a high voltage level and the second controlling signal is at a low voltage level; when the following frame of image is displayed, the second controlling signal is at a high voltage level and the first controlling signal is at a low voltage level.

14. The OLED pixel driving circuit of claim 13, wherein the first controlling signal and the second controlling signal are both signals with a square wave; the period of the first controlling signal is the same as the period of the second controlling signal; the polarity of the first controlling signal is opposite to the polarity of the second controlling signal.

15. The OLED pixel driving circuit of claim 11, wherein the first data signal and the second data signal are set according to the brightness of the first OLED and the brightness of the second OLED at the same grayscale level; the brightness of the first OLED is the same as the brightness of the second OLED at the same grayscale level.

16. The OLED pixel driving circuit of claim 8, wherein the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT, and the sixth TFT all are low temperature polysilicon TFTs, oxide semiconductor TFTs, or amorphous silicon (a-Si) TFTs arbitrarily.

17. An organic light emitting diode (OLED) display, comprising an OLED pixel driving circuit, the OLED pixel driving circuit comprising:

a first thin-film transistor (TFT), a second TFT, a third TFT, a fourth TFT, a fifth TFT, a sixth TFT, a capacitor, a first OLED, and a second OLED;

a gate of the first TFT receiving a scanning signal; a source of the first TFT receiving a data signal; a drain of the first TFT connected to a gate of the second TFT and one terminal of the capacitor;

a source of the second TFT and the other terminal of the capacitor both receiving a power supply positive voltage; a drain of the second TFT connected to a source of the third TFT and a source of the fifth TFT;

a gate of the third TFT, a gate of the fourth TFT, a gate of the fifth TFT, and a gate of the sixth TFT all receiving a controlling signal; a drain of the third TFT connected to an anode of the first OLED, a cathode of the second OLED, and a source of the sixth TFT;

a drain of the fifth TFT connected to a cathode of the first OLED, an anode of the second OLED, and a source of the fourth TFT;

a drain of the sixth TFT and a drain of the fourth TFT both receiving a power supply negative voltage.

18. The OLED display of claim 17, wherein the first TFT, the second TFT, the third TFT, and the fourth TFT are all N-type TFTs; the fifth TFT and the sixth TFT are both P-type TFTs.

19. The OLED display of claim 17, wherein when a current frame of image is displayed, the controlling signal is at a high voltage level; when a following frame of image is displayed, the controlling signal is at a low voltage level.

20. The OLED display of claim 17, wherein the OLED pixel driving circuit further comprises a seventh TFT and an eighth TFT; the controlling signal comprises a first controlling signal and a second controlling signal; the data signal comprises a first data signal and a second data signal;

a gate of the seventh TFT receives the first controlling signal; a source of the seventh TFT receives the first data signal;

a gate of the eighth TFT receives a second controlling signal; a source of the eighth TFT receives a second data signal; the source of the first TFT is connected to a drain of the seventh TFT and a drain of the eighth TFT;

the gate of the third TFT and the gate of the fourth TFT both receive the first controlling signal;

the gate of the fifth TFT and the gate of the sixth TFT T6 both receive the second controlling signal.

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摘要(译)

提供了一种有机发光二极管 (OLED) 像素驱动电路和OLED显示器。 OLED像素驱动电路包括第一薄膜晶体管 (TFT) , 第二TFT, 第三TFT, 第四TFT, 第五TFT, 第六TFT, 电容器, 第一OLED和第二OLED。 第三TFT的漏极连接到第一OLED的阳极, 第二OLED的阴极和第六TFT的源极。 第五TFT的漏极连接到第一OLED的阴极, 第二OLED的阳极和第四TFT的源极。 第六TFT的漏极和第四TFT的漏极均接收电源负电压。

